VARIABLE FIXED MULTIPLIERS USING MEMORY BLOCKS

ABSTRACT OF THE INVENTION

A programmable logic device includes at least one RAM block generating a first multi-bit calculation result which may, but does not necessarily, involve a multiplication of two operands. A shift operation is driven by a second multi-bit calculation result shifts the second multi-bit calculation result by at least one bit to generate a shifted second multi-bit calculation result. A multi-bit adder coupled to the at least one RAM block adds the shifted second multi-bit calculation result to the first multi-bit calculation result.